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Assessment of performance with the Comparision of Asymmetrical Cascaded and Reduced Switch Multilevel Inverter of Space Vector Control Modulation

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Abstract: In recent research activities, different types of multilevel inverters are designed to fulfil the present requirements of power. Already some of the standard multilevel inverters take major role in the electrical market like, Diode Clamped, Flying Capacitor and Cascaded H-Bridge multilevel inverter. In cascaded type, Asymmetrical multilevel inverter is most popular one; but different types of multilevel inverters are introduced with the capabilities of reduced switches, reduced number of sources, single DC source and single bridge etc. In this paper comparision of reduced switch multilevel inverter with standard asymmetrical cascaded multilevel inverter to analyze the various aspects like implementation, performance, applications and computational complexity. This analysis gives the idea about recently introduced multilevel inverters among the standard inverters.

Keywords: Asymmetrical Multilevel Inverter, Reduced Switch Multilevel Inverter, Space Vector Control Modulation, Total Harmonic Distortion, Pulse Generation.

I. INTRODUCTION

In last decade, research impact on multilevel inverters is high and they are elevated in application oriented research with the implementation flexibility. At present some of the standard multilevel inverters are designed bulky in amount with different manufacturers for the commercial purpose, among those inverters, asymmetrical cascaded multilevel inverter growth is high at the present scenario. So many numbers of multilevel inverters are introduced in recent times and itself they are the best ones like exposed by the introducers. In the comparative analysis of recently developed reduced switch multilevel [1] is evaluated with the performance of standard Asymmetrical Multilevel Inverter.

A. Asymmetrical Cascaded Multilevel Inverter

Asymmetrical cascaded multilevel inverter's block diagram is shown in Fig. 1. In the topology the multilevel inverter has the cascaded H-bridge with the different dc voltage ratios of a particular policy to get more number of voltage levels with the same rugged construction of bridge for the high voltage applications [2].

The asymmetrical inverter consists of full bridge conversion cells as like cascaded, quasi-linear, Hybrid multilevel inverter. However the DC link voltage along with the cells (N) has the relationship of 1V, 3V, 9V…3^{N-1}V. Due to this feature the level (*l*) of the output waveform for this topology equals to 3^N. So asymmetrical converter output voltage waveform for N = 3 it has 27 levels.

For this topology 12 switches and three asymmetrical voltage sources placed to operate in a specified manner. The maximum output voltage of this N cascaded multilevel inverter is Vo,Max= $((3^N-1)/2)V_{DC}$ [3-5].

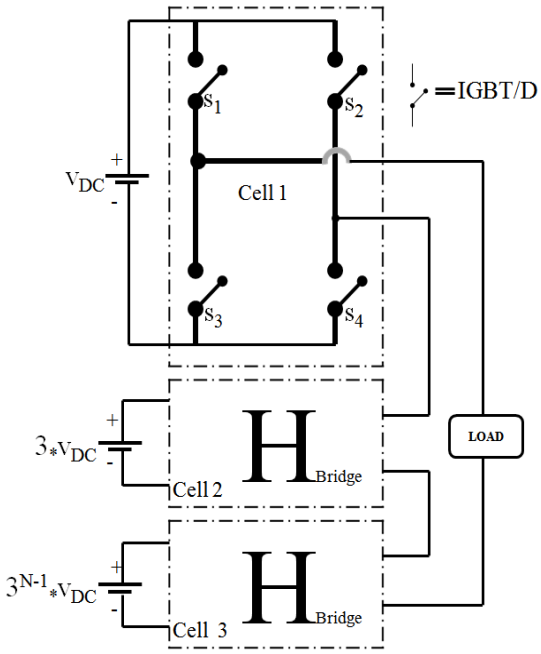

Fig.1.Asymmetrical Cascaded Multilevel Inverter Topology.

The switching state and the respective output voltage levels are shown in Table 1.

B. Reduced Switch Multilevel Inverter [1]

Reduced switch multilevel inverter is the newly introduced [1] got more research impact in the recent time. This multilevel inverter has no bridge configuration in its

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TABLE 1 SWITCHING STATES OF ASYMMETRICAL CASCADED MULTILEVEL INVERTER.

Voltage Level	Active DC Sources	Switching States of Switches											
		1	2	3	4	5	6	7	8	9	10	11	12
0	---	0	0	0	0	0	0	0	0	0	0	0	0
+1	1	1	0	0	1	0	0	1	1	0	0	1	1
+2	3-1	0	1	1	0	1	0	0	1	0	0	1	1
+3	3	0	0	1	1	1	0	0	1	0	0	1	1
+4	3+1	1	0	0	1	0	1	1	0	0	0	1	1
+5	9-3-1	0	1	1	0	0	1	1	0	1	0	0	1
+6	9-3	0	0	1	1	0	1	1	0	1	0	0	1
+7	9-3+1	1	0	0	1	0	0	1	1	1	0	0	1
+8	9-1	0	1	1	0	0	0	1	1	1	0	0	1
+9	9	0	0	1	1	0	0	1	1	1	0	0	1
+10	9+1	1	0	0	1	0	0	1	1	1	0	0	1
+11	9+3-1	0	1	1	0	1	0	0	1	1	0	0	1
+12	9+3	0	0	1	1	1	0	0	1	1	0	0	1
+13	9+3+1	1	0	0	1	1	0	0	1	1	0	0	1

TABLE 2 SWITCHING STATES OF REDUCED SWITCH MULTILEVEL INVERTER.

Voltage Level	Active DC Sources	Switching States of Switches									
		1	2	3	4	5	6	7	8	9	10
0	---	1	0	1	0	1	0	1	0	1	0
+1	1	1	0	0	1	0	1	0	1	0	1
+2	2	0	1	0	1	1	0	0	1	0	1
+3	2+1	1	0	0	1	1	0	0	1	0	1
+4	5-1	0	1	1	0	0	1	0	1	0	1
+5	5	1	0	1	0	0	1	0	1	0	1
+6	5+1	0	1	1	0	1	0	0	1	0	1
+7	5+2	1	0	1	0	1	0	0	1	0	1
+8	5+2+1	0	1	0	1	0	1	1	0	0	1
+9	10-1	1	0	0	1	0	1	1	0	0	1
+10	10	0	1	0	1	1	0	1	0	0	1
+11	10+1	1	0	0	1	1	0	1	0	0	1
+12	10+2	0	1	1	0	0	1	1	0	0	1
+13	10+2+1	1	0	1	0	0	1	1	0	0	1
+14	10+5-1	0	1	1	0	1	0	1	0	0	1
+15	10+5	1	0	1	0	1	0	1	0	0	1

topology. The structure of the inverter looks like a sequential switches and meshed dc sources. 31 level reduced switch multilevel inverter topology is shown in Fig.2. In this configuration of inverter the voltage sources has no relation and no strategic approach to allot the voltage values, by the topology and the feasible

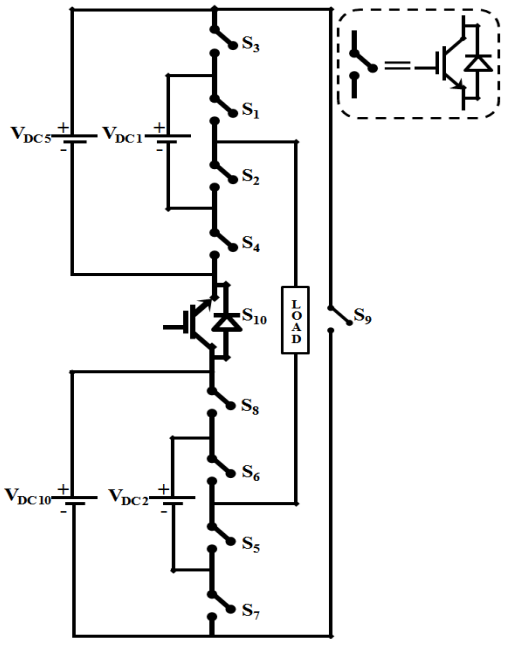

Fig.2. Reduced switches Multilevel Inverter [1].

approach to conduct the path for the specific operation only decides the values of voltage sources [6]. Above shown topology of inverter having four voltage sources and 10 switches to get a 31 level output. The switching state with respect to level of output are tabulated in Table2 Section I.A and I.B gives the short and clean idea about the configuration, operation and switching states for the various levels are described. These two multilevel inverters are modulated with the Space Vector Control Strategy, the implementation and operating methodology was concise in Section II.

II. SPACE VECTOR CONTROL MODULATION

Space vector control strategy [7] is a simple and the best modulation strategy over the others in the sample or time based operating systems. The basic scheme is to take advantages of the more number of voltage vectors generated by a multilevel converter by simply approximating the reference to the closest voltage that can be generated in the d-q plane, without even requirement of modulation.

Therefore, this strategy is specified as Space vector control instead of modulation. The operating principle of SVC is shown in Fig. 3, where the state-space vectors for 11-level inverter are illustrated, with a zoom to the NVC operating principle. Each dot is one of the feasible voltage vectors generated by the inverter; they are surrounded by a hexagon that indicates the boundary of the area in they are the closest available voltage vectors.

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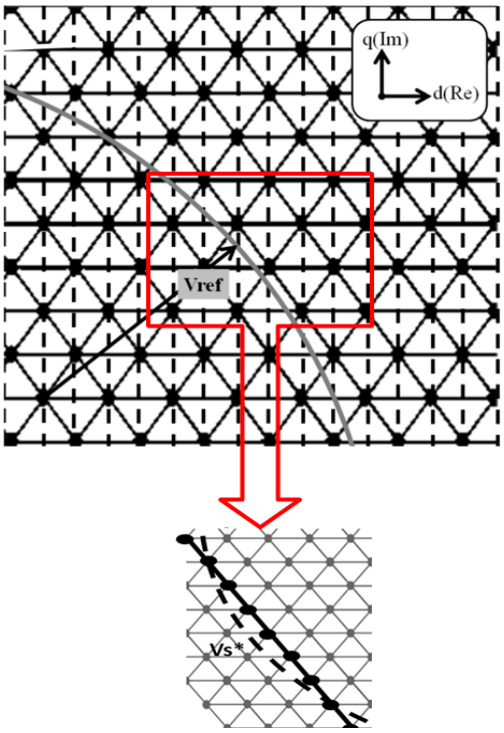

Fig.3. Operating Logic for NVC.

The dashed line shown in Fig. 3 is the voltage space vector reference (Vs*) trajectory through the complex plane. Hence, when the reference falls into a certain hexagon, the corresponding vector will be generated by the inverter. The selected vector is illustrative with respect to the SVC strategy [8-10] and is shown in zoomed part of Fig. 3.
This strategy having less complexity in computations when operates the plant, moreover it need to follow the reference to pick up the required state of operation to generate specified level in output.

III. SIMULATION RESULTS AND ANALYSIS

Overview of the topology and the configuration of operating patterns gives some of the variations between the asymmetrical cascaded and reduced switch multilevel, in this the main variations is only the topology. Based on the topology only the dc voltages are varies, number of switches are reduced in reduced switch multilevel inverter but one more source is added with the comparision of standard asymmetrical multilevel inverter.

The output voltage and current waveforms of a reduced switch and asymmetrical cascaded multilevel inverters are shown in Figs. 4 & 5 respectively.

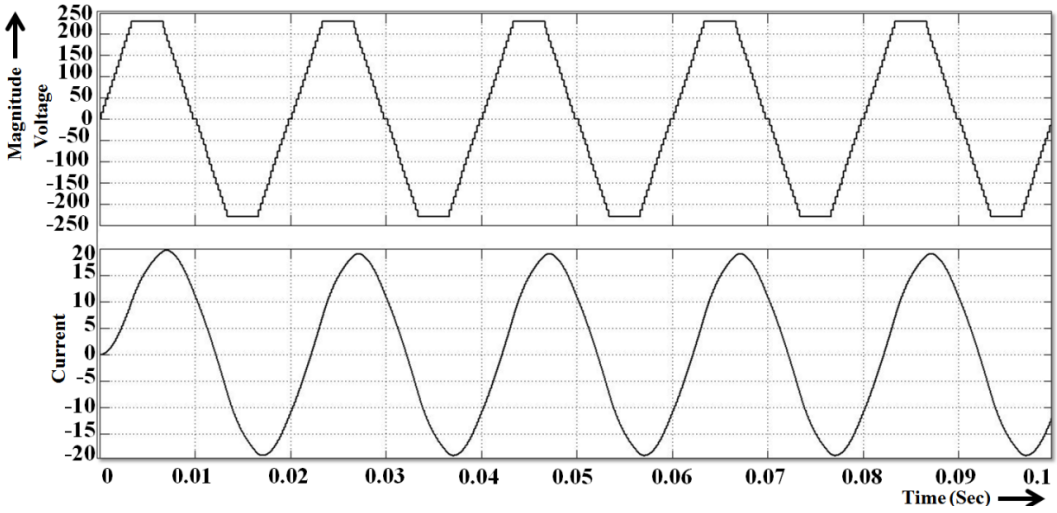

Fig.4. Voltage and Current wave forms of Reduced Switch Multilevel Inverter.

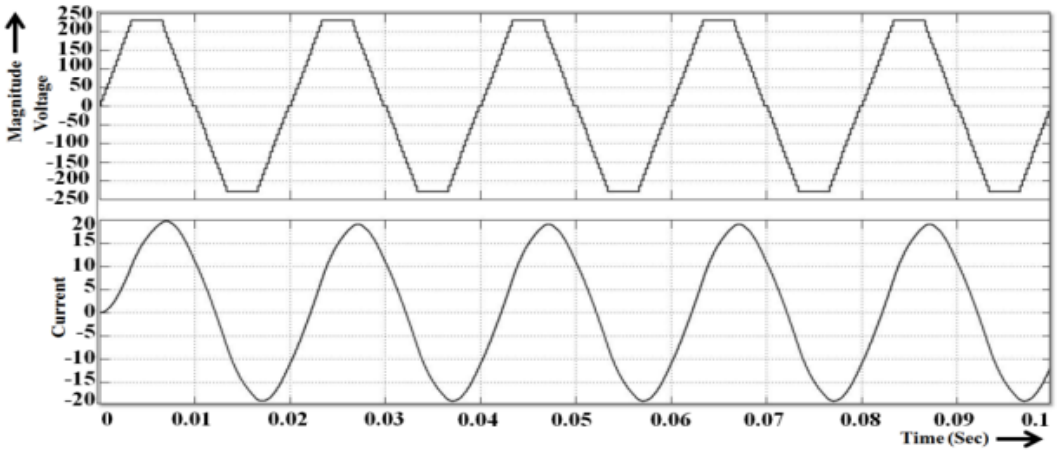

Fig. 5. Voltage and Current wave forms of Asymmetrical cascaded Multilevel Inverter.

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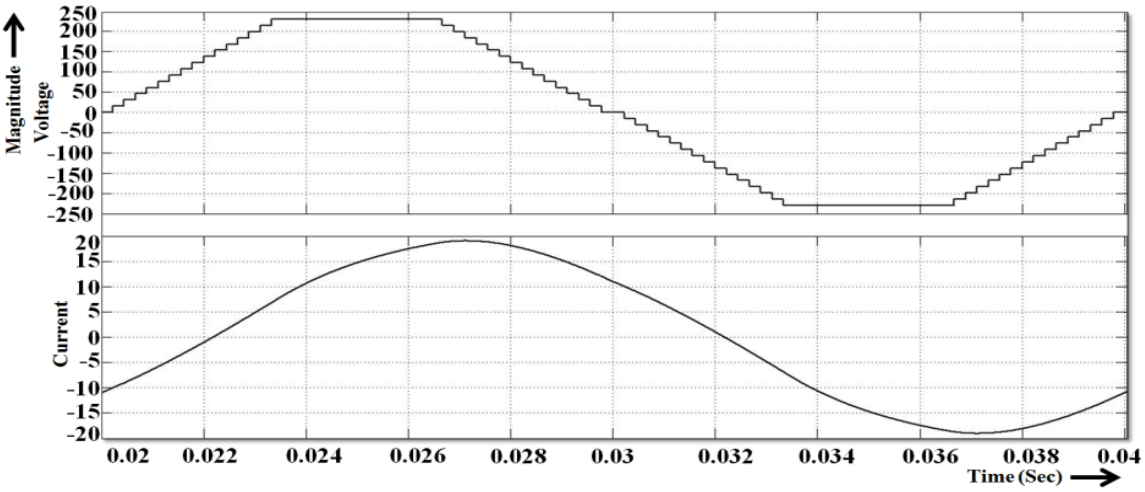

Fig.6. One Cycle of Voltage and Current wave forms of Reduced Switch Multilevel Inverter.

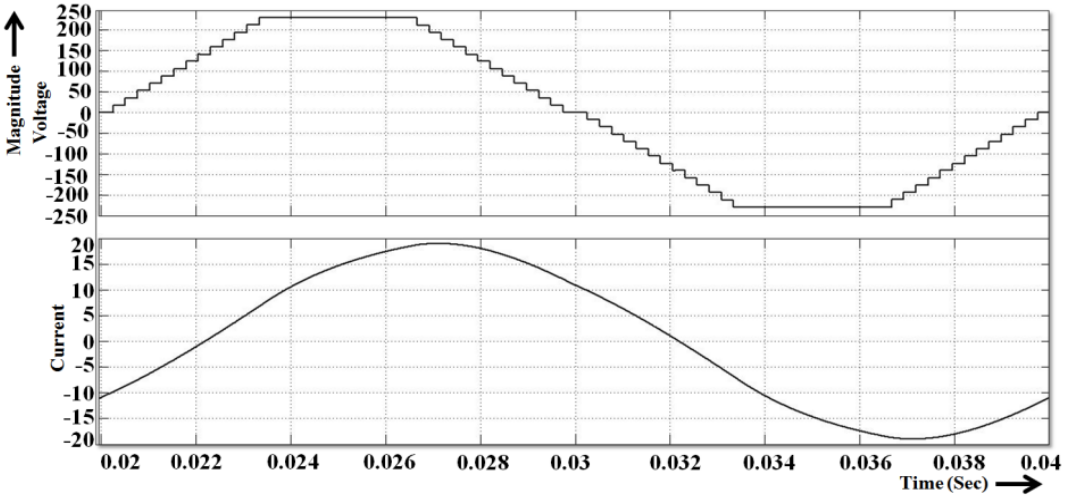

Fig. 7. One Cycle of Voltage and Current wave forms of Asymmetrical Cascaded Multilevel Inverter.

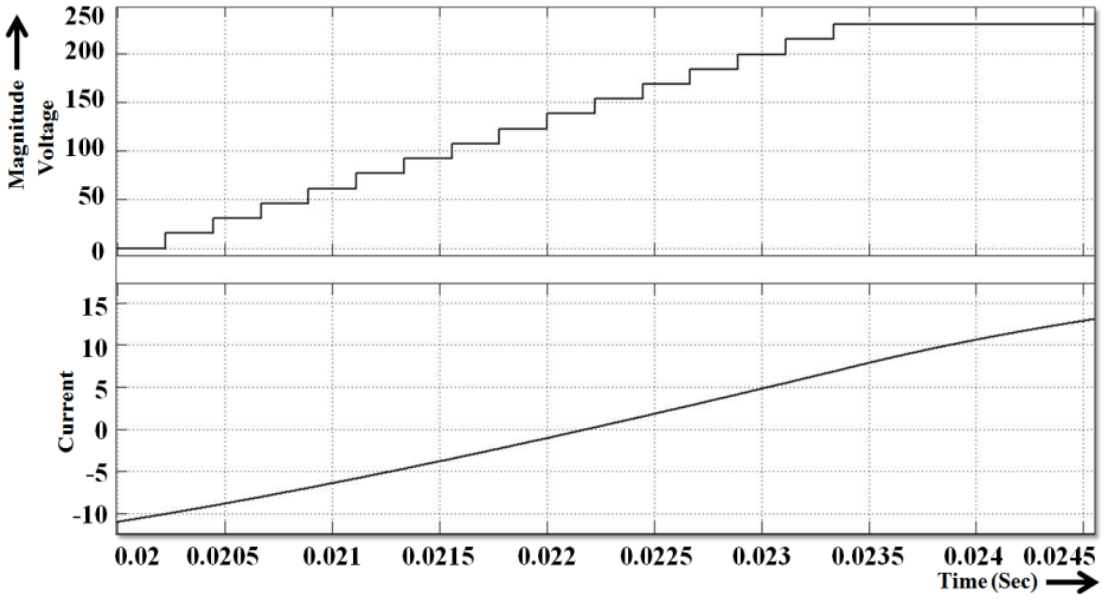

Fig.8. Clear view of level of Voltage and Current wave forms of Reduced Switch Multilevel Inverter.

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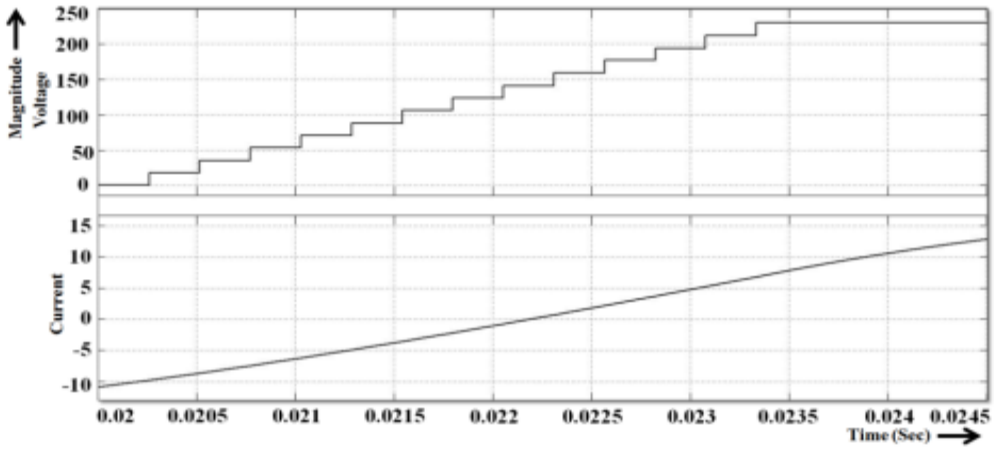

Fig.9. Clear view of level of Voltage and Current wave forms of Asymmetrical Cascaded Multilevel Inverter.

The clear view of levels with reduced switch and asymmetrical cascaded multilevel inverter is illustrated in Figs. 8 & 9 respectively.

TABLE 3 PERFORMANCE PARAMETERS OF REDUCED SWITCH AND ASYMMETRICAL CASCADED MULTILEVEL INVERTER.

Type of Multilevel Inverter	No. of Switches	No. of Voltage Sources	No. of Levels	V_{THD} (%)	Fundamental Voltage Value (V)	I_{THD} (%)	Fundamental Current Value (A)
Reduced Switch	10	4	31	6.17	237.1	2.01	18.65
Asymmetrical cascaded	12	3	27	6.58	236.2	2.19	18.57

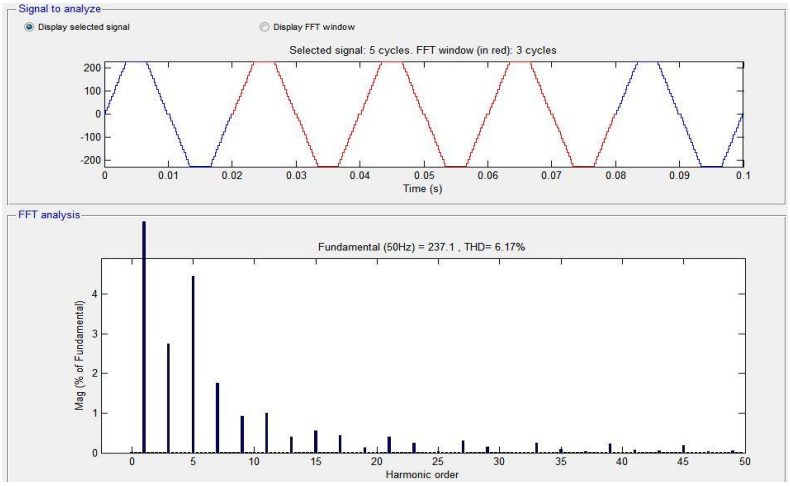

Fig.10. FFT Analysis for Voltage signal for Reduced Switch Multilevel Inverter.

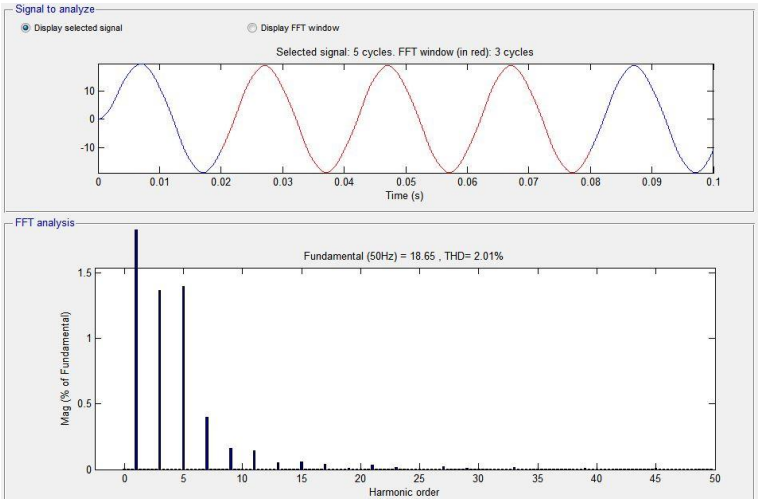

Fig.11. FFT Analysis for Current signal for Reduced Switch Multilevel Inverter.

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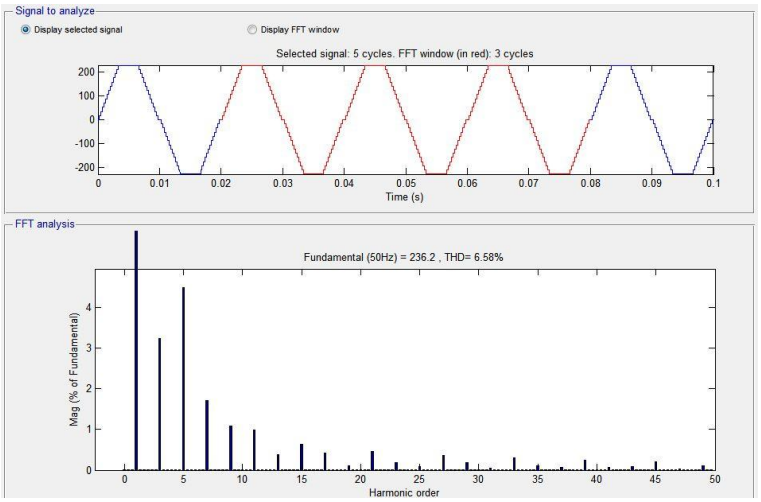

Fig.12. FFT Analysis for Voltage signal for Asymmetrical Cascaded Multilevel Inverter.

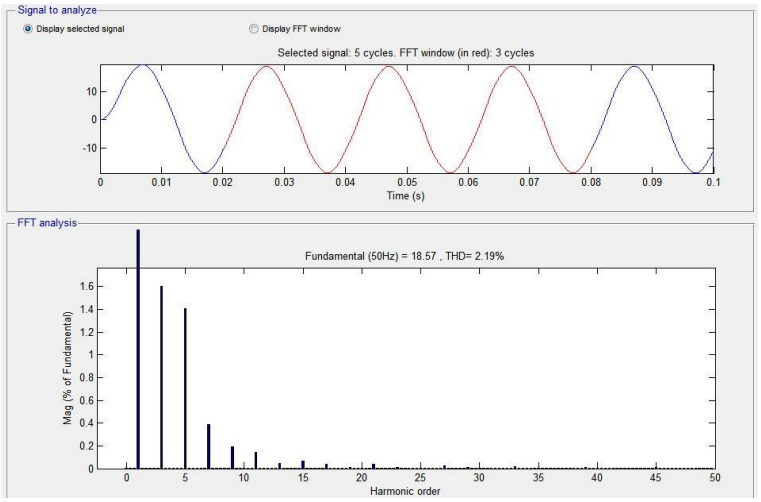

Fig. 13. FFT Analysis for Current signal for Asymmetrical Cascaded Multilevel Inverter.

In Fig. 6 the output voltage levels are 31 and it is with the reduced switch topology, because of four dc voltage sources are used but two switches are reduced with the reference of standard asymmetrical cascaded multilevel inverter. 27 level output voltage of asymmetrical cascaded multilevel inverter is shown in Fig. 7.

Voltage and current's total harmonic distortions values indicates the performance of the inverters and the V_{THD} and I_{THD} of the reduced switch multilevel inverter is shown in Figs. 10 & 11 respectively, similarly asymmetrical cascaded multilevel inverter is shown in 12 & 13 respectively. The total performance parameters are tabulated in Table 3, for the easy comparision of these two multilevel inverters.

IV. CONCLUSION

As per the discussion on previous sections, simulated and physical performance parameters of the reduced switch and asymmetrical cascaded multilevel inverters are analysed and concluded that the both inverters are having the same number of advantages and disadvantages also. The number of sources are high in reduced switch and more number of switches in asymmetrical inverter, as well THD parameters are also same for the both inverters but reduced switch having less THD but comparatively it has more number of levels because of its topology, even though comparatively both are having the same THD and fundamental values. In practical implementation point of view cascaded inverter is well known to manufacturers but reduced switch inverter is not, moreover installation and maintenance of switch is very easy than batteries, so finally Asymmetrical Cascaded Multilevel Inverter is the better one among the others.

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